In re Patent Application of:
SONZOGNI ET AL.
Serial No. **09/914,315**
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In the Claims:

Claims 1-4 (Previously Cancelled).

5. (Currently Amended) A chip card comprising:

a microprocessor including an operating system working with a set of instructions, said microprocessor comprising a first register for storing a ~~first~~ multibit identification code identifying ~~code, on at least one check bit, for~~ an entity to be executed, the set of instructions including a call instruction for calling based upon the multibit identification code a new entity to be executed, and for updating said first register during execution of the new entity by storing therein a first label associated with the entity being executed; ~~said first register being updated based upon a call instruction and a return instruction during execution of a new entity;~~

a memory connected to said microprocessor for storing a plurality of application programs; ~~and~~

a first link connected to said microprocessor for transmitting the multibit identification code; and

a checking device connected to said first link ~~microprocessor~~ for receiving the multibit identification code, and for checking ~~checking, as a function of the at least one check bit,~~ whether access to locations in said memory is authorized for the new entity ~~entity.~~ by comparing the first label with a second label, the second label being associated with the plurality of application programs in said memory or with the locations in said memory, and the second label also being used for initiating reading of one of said plurality of application programs therein.

6. (Currently Amended) A chip card according to Claim 5, wherein the set of instructions further includes a return instruction; and wherein said microprocessor comprises a second register and ~~register for storing a second code for the application programs active when a last call instruction was sent~~ loads the multibit identification code from said first register to said second register when the call instruction is executed, and at a same time the return instruction causes the contents of said second register to be loaded into said first register.

7. (Currently Amended) A chip card according to Claim 6, wherein said second register ~~can not~~ cannot be directly accessed.

8. (Currently Amended) A chip card according to Claim 5, wherein ~~each~~ the new entity to be executed is one of the plurality of application programs.

9. (Currently Amended) A chip card according to Claim 5, wherein ~~each~~ the new entity to be executed causes a hardware event.

10. (Previously Added) A chip card according to Claim 9, wherein the hardware event resets said microprocessor.

11. (Currently Amended) A chip card according to Claim 5, wherein the set of instructions further includes a

return instruction; and wherein said first register is updated in response to the return instruction.

12. (Currently Amended) A chip card according to Claim 5, wherein said checking device provides a control signal to said microprocessor for providing access to the locations ~~of~~ in said memory if the new entity to be executed is authorized.

13. (Currently Amended) A chip card according to Claim 5, wherein the plurality of application programs are written in a standardized language ~~said checking device compares the address locations to be accessed in said memory and the first code in said first register~~.

14. (Previously Added) A chip card comprising:

~~a microprocessor comprising~~

~~a first register for storing a first code, on at least one check bit, for an application program to be executed, said first register being updated based upon a call instruction and a return instruction during execution of a new application program, and~~

~~a second register for storing a second code for an application program active when a last call instruction was sent;~~

a microprocessor including an operating system working with a set of instructions including a call instruction and a return instruction, said microprocessor comprising

a first register for storing a multibit identification code identifying an application program entity to be executed, the call instruction for calling based upon the multibit identification code a new application program to be executed, and for updating said first register during execution of the new application program by storing therein a first label associated with the application program being executed, and

a second register for loading the multibit identification code from said first register to said second register when the call instruction is executed, and at a same time the return instruction causes the contents of said second register to be loaded into said first register;

a memory connected to said microprocessor for storing ~~the~~ a plurality of application programs; ~~program;~~ and

~~a checking device connected to said microprocessor for checking, as a function of the at least one check bit, whether access to locations in said memory is authorized for the new application program, said checking device providing a control signal to said microprocessor for providing access to the locations of said memory if the new application program is authorized.~~

a checking device connected to said microprocessor for receiving the multibit identification code, and for checking whether access to locations in said memory is authorized for the new application program by comparing the first label with a second label, the second label being associated with the plurality of application programs in said

memory or with the locations in said memory, and the second label also being used for initiating reading of one of said plurality of application programs therein.

15. (Currently Amended) A chip card according to Claim 14, wherein said second register ~~can not~~ cannot be directly accessed.

16. (Previously Added) A chip card according to Claim 14, wherein each application program causes a hardware event.

17. (Previously Amended) A chip card according to Claim 16, wherein the hardware event resets said microprocessor.

18. (Previously Added) A chip card according to Claim 14, wherein said first register is automatically updated in response to the return instruction.

19. (Previously Added) A chip card according to Claim 14, wherein said checking device provides a control signal to said microprocessor for providing access to the locations in said memory if the new application program to be executed is authorized ~~said checking device compares the address locations to be accessed in said memory and the first code in said first register~~.

20. (Currently Amended) A method for securing access to a chip card comprising a microprocessor including an

operating system working with a set of instructions including a call instruction, and a memory connected to the microprocessor for storing a plurality of application programs, the method comprising:

~~storing a first code, on at least one check bit, in a first register of the microprocessor for an entity to be executed;~~

~~updating the first register based upon a call instruction and a return instruction during execution of a new entity; and~~

~~checking, as a function of the at least one check bit, whether access to locations in the memory is authorized for the new entity.~~

storing a multibit identification code in a first register identifying an entity to be executed;

calling a new entity to be executed based upon the multibit identification code stored in the first register;

updating the first register during execution of the new entity by storing therein a first label associated with the entity being executed; and

transmitting the multibit identification code from the microprocessor to a checking device, and checking whether access to locations in the memory is authorized for the new entity by comparing the first label with a second label, the second label being associated with the plurality of application programs in the memory or with the locations in the memory, and the second label also being used for reading one of the plurality of application programs therein.

21. (Currently Amended) A method according to Claim

20, ~~further comprising storing a second code in a second register of the microprocessor for an application program active when a last call instruction was sent.~~ wherein the set of instructions further includes a return instruction; and wherein the microprocessor comprises a second register and loads the multibit identification code from the first register to the second register when the call instruction is executed, and at a same time the return instruction causes the contents of the second register to be loaded into the first register.

22. (Currently Amended) A method according to Claim 21, wherein the second register ~~can not~~ cannot be directly accessed.

23. (Currently Amended) A method according to Claim 20, wherein ~~each~~ the new entity to be executed is one of the plurality of application programs.

24. (Currently Amended) A method according to Claim 20, wherein ~~each~~ the new entity to be executed causes a hardware event.

25. (Previously Added) A method according to Claim 24, wherein the hardware event resets the microprocessor.

26. (Currently Amended) A method according to Claim 20, wherein the set of instructions further includes a return instruction; and wherein the first register is updated in response to the return instruction.

27. (Currently Amended) A method according to Claim 20, wherein the checking comprises providing a control signal to the microprocessor for providing access to the locations ~~of~~ in the memory if the new entity to be executed is authorized.

28. (Currently Amended) A method according to Claim 20, wherein the plurality of application programs are written in a standardized language ~~checking comprises comparing the address locations to be accessed in the memory and the first code in the first register~~.

29. (Currently Amended) A method for securing access to a chip card comprising a microprocessor and a memory connected thereto for storing a plurality of application programs, the microprocessor including an operating system working with a set of instructions including a call instruction and a return instruction, the method comprising:

~~storing a first code, on at least one check bit, in a first register of the microprocessor for an application program to be executed;~~

~~updating the first register based upon a call instruction and a return instruction during execution of a new application program; and~~

~~checking, as a function of the at least one check bit, whether access to locations in the memory is authorized for the new application program.~~

storing a multibit identification code in a first register for identifying an application program to be executed;

calling a new application program to be executed

based upon the multibit identification code;

updating the first register during execution of the new application program by storing therein a first label associated with the application program being executed;

loading the multibit identification code from the first register to a second register when the call instruction is executed, and at a same time the return instruction causes the contents of the second register to be loaded into the first register; and

transmitting the multibit identification code from the microprocessor to a checking device for checking whether access to locations in the memory is authorized for the new application program by comparing the first label with a second label, the second label being associated with the plurality of application programs in the memory or with the locations in the memory, and the second label also being used for initiating reading of one of the plurality of application programs therein.

Claim 30 (Cancelled.)

31. (Currently Amended) A method according to Claim 29, wherein the second register ~~can not~~ cannot be directly accessed.

32. (Previously Added) A method according to Claim 29, wherein each application program causes a hardware event.

33. (Previously Amended) A method according to Claim 32, wherein the hardware event resets the microprocessor.

34. (Previously Added) A method according to Claim 29, wherein the first register is updated in response to the return instruction.

35. (Previously Added) A method according to Claim 29, wherein checking comprises providing a control signal to the microprocessor for providing access to the locations of the memory if the new application program is authorized.

Claim 36 (Cancelled.)

37. (Previously Added) A chip card comprising:

a microprocessor;

a memory connected to said microprocessor for storing a plurality of application programs;

said microprocessor comprising a first register for storing a first code, on at least one check bit, corresponding to a first application program to be executed from said plurality of application programs;

if execution of said first application program requires intervention of a second application program from said plurality of application programs, then said first application program sends a call instruction to said microprocessor requesting such intervention;

said first register being updated based upon the call instruction for storing a second code, on the at least one check bit, corresponding to said second application program to be executed; and

a checking device connected to said microprocessor

for checking the second code as to whether access to locations in said memory are authorized for said second application program.

38. (Previously Added) A chip card according to Claim 37, wherein said microprocessor comprises a second register for storing the first code corresponding to said first application program while said second application program is being executed; said first register also being updated based upon the first code.

39. (Previously Added) A chip card according to Claim 38, wherein after said microprocessor executes said second application program, said first register enables said microprocessor to return to said first application program.

40. (Currently Amended) A chip card according to Claim 38, wherein said second register ~~can not~~ cannot be directly accessed.

41. (Previously Added) A chip card according to Claim 37, wherein said first and second application programs are written in a standardized language.

42. (Previously Added) A chip card according to Claim 41, wherein said first and second application programs are loaded into said memory after the chip card has been fabricated.

43. (Previously Added) A chip card according to

Claim 37, wherein said checking device provides a control signal to said microprocessor for providing access to the locations of said memory if said second application program is authorized.

44. (Previously Added) A chip card according to Claim 37, wherein said checking device compares the address locations to be accessed in said memory with the second code in said first register.